

Technik & Architektur

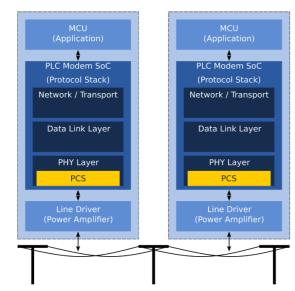
Information and Communication Technologies Master of Science in Engineering

Master-Thesis Information and Communication Technologies

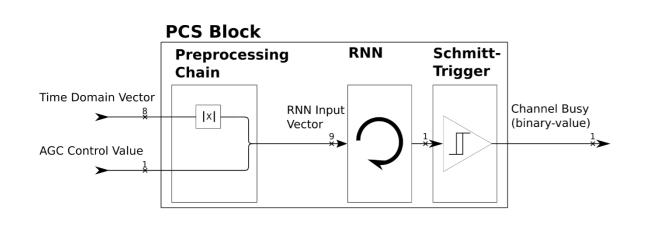
Powerline Communication with AI-based Physical Carrier Sensing

PCS Block Averaging Method (Existing Solution)

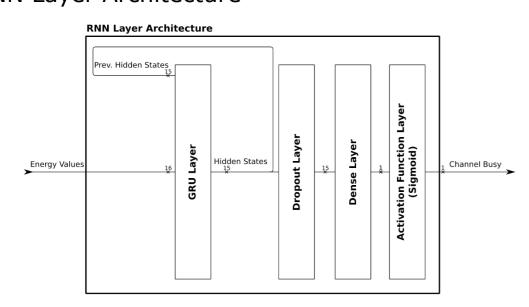
PLC System Overview



PCS Block Overview RNN

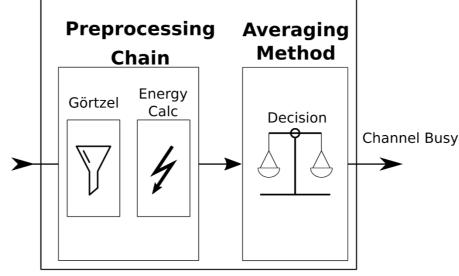


RNN Layer Architecture

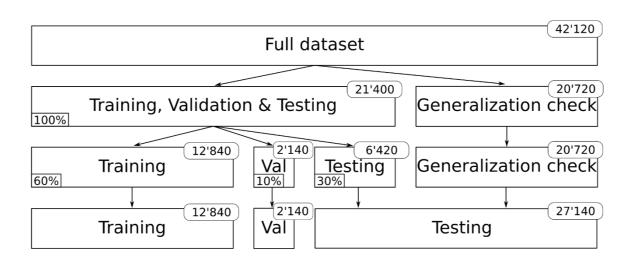


Verification example Flat-Fading with 30 dB chn. att. and AWGN with 12 dB SNR

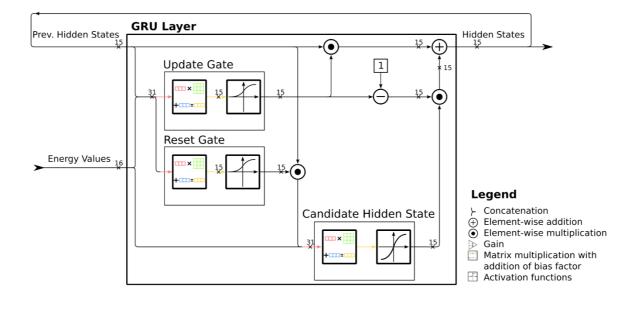
Görtzel



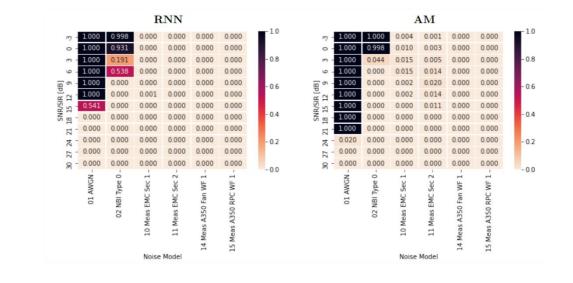
Training, Validation & Test Dataset



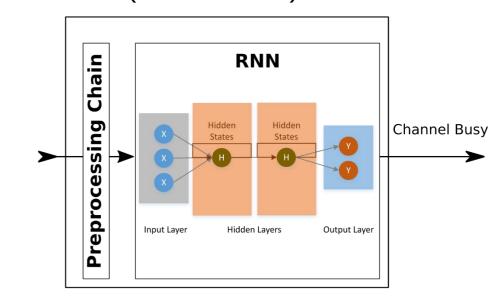
GRU Layer Architecture



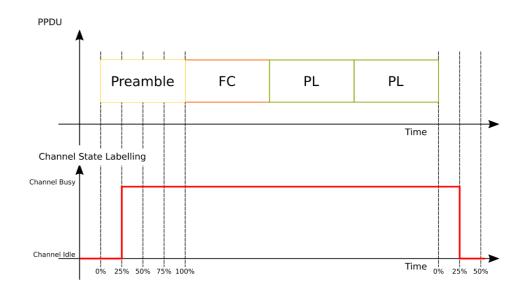
Error Rate from RNN in Hardware (left) and from Averaging Method (right)



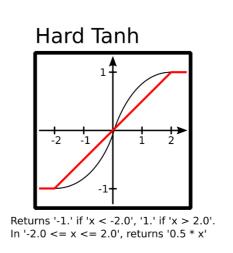
PCS Block RNN (New Solution)

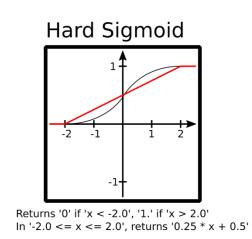


Dataset Labelling



Optimized Activation Functions Tanh & Sigmoid





Performance Averaging Method versus RNN



Task Identification

The use of Artificial Intelligence (AI) for a Power Line Communication (PLC) system with an Orthogonal Frequency-Division Multiplexing (OFDM) modulation scheme is investigated for Lucerne University of Applied Sciences and Arts (HSLU).

The present work target attempts to replace the existing Physical Carrier Sensing (PCS) block with a more robust implementation. The approach is to use AI in the PCS block. The new implementation with a Recurrent Neural Network (RNN) algorithm should be implemented in the Power Line Communication (PLC) system on a Field Programmable Gate Array (FPGA).

On the hardware platform, the RNN has to be optimized and adapted to the real-time requirements. The final implementation are compared with the existing implementation.

Conclusion / Summary

Firstly, the existing PCS implementation is analysed to elaborate a transformation from the theoretical RNN to an implementable solution.

Secondly, the elaborated PCS implementation is prepared for an implementation on a FPGA. The central part is to fulfil the timing requirements on the hardware and reach a sufficient throughput with the PCS block. The hardware architecture is implemented in Xilinx System Generator.

Thirdly, the PCS block with a RNN is tested on the test-bench from HSLU. To get a comprehensive comparison to the existing implementation, different test setups and test cases are set up. In iterative steps are the RNN optimized and improved for the hardware.

Finally, the RNN implementation detects stable data packets in real-time on various channel characteristics and noise scenarios.

Overall, it is shown that a RNN can solve such a task. The current implementation shows in many conditions better results than the averaging method.

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